C (Printed Pages 4)

Roll No.

21/1088

B.C.A. (Third Semester)

Examination, 2021

Third Paper

(Computer Architecture & Assembly Language)

Time : Three Hours] *[Maximum Marks : 75*

Note : Attempt any **five** questions. **All** questions carry equal marks. The answers to short answer type questions should not exceed 200 words and the answer to long answer type questions should not exceed 500 words.

1. Define and explain with an example: 3×5=15

   (a) Instruction cycle

   (b) Flag Register

   (c) Interrupt Handling

   (d) Special purpose registers

P.T.O.

   (e) Memory Read and Memory Write Instructions.

2. Write the format interpretation and method of execution of the following types of instructions: 5+5+5

   (a) Arithmetic Instructions

   (b) Logical Instructions

   (c) Register transfer operations

3. What is meant by memory interfacing? Explain the basic steps to be considered for performing memory interfacing. Also explain the difference between memory and I/o interfacing. 15

4. Write an explanatory note on the following: 15

   (a) General Register Organization

   (b) Addressing modes

Give suitable examples/diagram where necessary.

5. Explain the concept of RISC with example. How is it different from CISC? What are the relative advantages/disadvantages of each scheme? 15

6. State the elaborate Booth's algorithm and illustrate it with an example. 15

7. How are floating point numbers represented in computer memory? Explain the concept of

(a) Normalized floating point numbers

(b) Floating point multiplication

(c) Errors due to rounding off.

Give examples where necessary.

8. What is DMA? Explain its operation with the help of a clear schematic diagram. How is it superior to Programmed I/o scheme?

https://www.mgkvponline.com

https://www.mgkvponline.com

https://www.mgkvponline.com

https://www.mgkvponline.com

https://www.mgkvponline.com

9. For the Intel 8085 microprocessor, write an account on:

(a) Pin diagram of 8085 and the purpose of different pin-sets

(b) CPU architecture of 8085

(c) Bus structure of 8085