Question Booklet Number

OMR Answer Sheet No.

23/3193

B.C.A. (II Semester) Examination, 2023

Digital Electronics and Computer Organization (DECO)

Booklet Code **D**

Paper : II

(Major)

(निम्न पूर्तियाँ परीक्षार्थी स्वयं भरें / To be filled in by the Candidate)

अनुक्रमांक (अंकों में)
Roll No. (in figures) _____

[समय : 2 : 00 घण्टे
[Time : 2 : 00 Hours

अनुक्रमांक (शब्दों में)
Roll No. (in words) _____

[अधिकतम अंक : 75
[Maximum Marks : 75

Enrolment No. (in figures) _____

कॉलेज का नाम
Name of College _____

कक्ष निरीक्षक के हस्ताक्षर
Signature of Invigilator

परीक्षार्थियों के लिए निर्देश :

1. प्रश्न-पुस्तिका को तब तक न खोलें जब तक आपसे कहा न जाए।
2. इस प्रश्न-पुस्तिका में कुल 75 प्रश्न हैं। परीक्षार्थियों को सभी प्रश्न हल करना अनिवार्य है। दिये गये OMR उत्तर-पत्रक पर ही सभी प्रश्न हल करना है। सभी प्रश्नों के अंक समान हैं।
3. प्रश्नों के उत्तर अंकित करने से पूर्व प्रश्न-पुस्तिका तथा OMR उत्तर-पत्रक को सावधानीपूर्वक देख लें। दोषपूर्ण प्रश्न-पुस्तिका, जिसमें कुछ भाग छपने से छूट गये हों या प्रश्न एक से अधिक बार छप गये हों या किसी भी प्रकार की कमी हो, उसे तुरन्त बदल लें।

(शेष निर्देश अन्तिम पृष्ठ पर)

Instructions to the Examinee :

1. Do not open the booklet unless you are asked to do so.
2. This booklet contains 75 questions. Examinee have to attempt all questions. All questions attempt on the given OMR Answer Sheet. All questions carry equal marks.
3. Examine the Booklet and the OMR Answer-Sheet very carefully before you proceed. Faulty question booklet due to missing or duplicate pages/questions or having any other discrepancy should be immediately replaced.

(Remaining Instructions on last page)

1. How many inputs will a decimal-to-BCD encoder have?

(1) 4

(2) 8

(3) 10

(4) 16

2. How many outputs will a decimal-to-BCD encoder have?

(1) 4

(2) 8

(3) 12

(4) 16

3. Which method of combination circuit implementation is widely adopted with maximum output functions and minimum requirement of ICs?

(1) Multiplexer Method

(2) Decoder Method

(3) Encoder Method

(4) Parity Generator Method

4. What is the normal operating condition of decoder corresponding to input & output states?

(1) E=0 & Outputs at '0' logic state

(2) E=1 & Outputs at '1' logic state

(3) E=0 & Outputs at '1' logic state

(4) E=1 & Outputs at '0' logic state

5. A counter is fundamentally a _____ sequential circuit that proceeds through the predetermined sequence of states only when input pulses are applied to it.

(1) register

(2) memory unit

(3) flip-flop

(4) arithmetic logic unit

6. Match the following sequential Circuits with associated functions:

1. Counter	A.	Storage of Program & data in a digital computer
2. Register	B.	Generation of timing variables to sequence the digital system operations
3. Memory	C.	Design of Sequential Circuits

Codes :

(1) 1-A, 2-B, 3-C

(2) 1-C, 2-B, 3-A

(3) 1-C, 2-A, 3-B

(4) 1-B, 2-C, 3-A

7. What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?

(1) 0 to 2^n

(2) 0 to 2^{n-1}

(3) 0 to 2^{n+1}

(4) 0 to $2^{n+1/2}$

8. A hard disk with 20 surfaces will have ___ heads.

(1) 10

(2) 05

(3) 01

(4) 20

9. The set of corresponding tracks on all the surfaces of a Hard Disk form a:

(1) Track Set

(2) Cylinder

(3) Cluster

(4) Block

10. The _____ process divides the disk into sectors and tracks.

(1) Updation

(2) Creation

(3) Initialization

(4) Formating

11. The Disk Access time is composed of:

(1) Seek Time

(2) Rotational Delay

(3) Latency Time

(4) Both Seek Time and Rotational Delay

12. The Disk Drive is connected to the system by the :

(1) PCI Bus

(2) SCSI Bus

(3) HDMI

(4) None of the mentioned

13. _____ is used to deal with the difference in data transfer rates between the Disk drive and the bus:

(1) Hubs

(2) Repeaters

(3) Data Buffers

(4) None of the mentioned

14. In a J-K Flip Flop the function K=J' is used to realize:

(1) T-Flip-Flop

(2) S-R Flip-Flop

(3) D-Flip-Flop

(4) M/S J-K Flip-Flop

15. The program is divided into parts called as

(1) Frames

(2) Segments

(3) Pages

(4) Sheets

16. The techniques which move the program blocks to or from the physical memory is called as ...

(1) Paging

(2) Virtual memory organisation

(3) Overlays

(4) Framing

17. _____ translates the logical address into a physical address

(1) MMU

(2) Translator

(3) Compiler

(4) Linker

18. In FIFO page replacement algorithm, when a page must be replaced

(1) oldest page is chosen

(2) newest page is chosen

(3) random page is chosen

(4) none of the mentioned

19. When a program tries to access a page that is mapped in address space but not loaded in physical memory, then _____

(1) segmentation fault occurs

(2) fatal error occurs

(3) page fault occurs

(4) no error occurs

20. Working set model for page replacement is based on the assumption of _____

(1) modularity

(2) locality

(3) globalization

(4) random access

21. Because of virtual memory, the memory can be shared among ____

(1) processes

(2) threads

(3) instructions

(4) none of the mentioned

22. The pager is concerned with the _____:

(1) individual page of a process

(2) entire process

(3) entire thread

(4) first page of a process

23. The Effective access time is directly proportional to ____

(1) page-fault rate

(2) hit ratio

(3) memory access time

(4) none of the mentioned

24. A process is thrashing if _____

(1) it is spending more time paging than executing

(2) it is spending less time paging than executing

(3) page fault occurs

(4) swapping can not take place

25. Which algorithm chooses the page that has not been used for the longest period of time whenever the page required to be replaced?

(1) first in first out algorithm

(2) additional reference bit algorithm

(3) least recently used algorithm

(4) counting based page replacement algorithm

26. _____ is the concept in which a process is copied into the main memory from the secondary memory according to the requirement.

(1) Paging

(2) Demand paging

(3) Segmentation

(4) Swapping

27. Segment replacement algorithms are more complex than page replacement algorithms because ____

(1) Segments are better than pages

(2) Pages are better than segments

(3) Segments have variable sizes

(4) Segments have fixed sizes

28. When a page fault occurs, the state of the interrupted process is ___

(1) disrupted

(2) invalid

(3) saved

(4) none of the mentioned

29. Virtual memory allows ____

(1) execution of a process that may not be completely in memory

(2) a program to be smaller than the physical memory

(3) a program to be larger than the secondary storage

(4) execution of a process without being in physical memory

30. A page fault occurs when:

(1) a page gives inconsistent data

(2) a page cannot be accessed due to its absence from memory

(3) a page is invisible

(4) all of the mentioned

31. The instruction being executed, must be in _____

(1) physical memory

(2) logical memory

(3) physical & logical memory

(4) none of the mentioned

32. Increasing the RAM of a computer typically improves performance because _____:

(1) Virtual memory increases

(2) Larger RAMs are faster

(3) Fewer page faults occur

(4) None of the mentioned

33. If no frames are free, _____ page transfer(s) is/are required.

(1) one

(2) two

(3) three

(4) four

34. Which of the following page replacement algorithms suffers from Belady's Anomaly?

(1) Optimal replacement

(2) LRU

(3) FIFO

(4) Both optimal replacement and FIFO

35. There are _____ cells in a 4-variable K-map.

(1) 12

(2) 16

(3) 18

(4) 8

36. The prime implicant which has at least one element that is not present in any other implicant is known as _____:

(1) Essential Prime Implicant

(2) Implicant

(3) Complement

(4) Prime Complement

37. Product-of-Sums expressions can be implemented using _____

(1) 2-level OR-AND logic circuits

(2) 2-level NOR logic circuits

(3) 2-level XOR logic circuits

(4) Both 2-level OR-AND and NOR logic circuits

38. Each group of adjacent Minterms (group size in powers of twos) corresponds to a possible product term of the given _____:

(1) Function

(2) Value

(3) Set

(4) Word

39. The output of a logic gate is 1 when all the input are at logic 0 as shown below :

INPUT		OUTPUT
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

The gate is ____

(1) A NAND

(2) An OR

(3) An AND

(4) A NOR,

40. The output of a logic gate is 1 when all the input are at logic 0 as shown below :

INPUT		OUTPUT
A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

The gate is _____

(1) an EX-OR

(2) an EX-NOR

(3) An AND

(4) A NOR

41. The following switching functions are to be implemented using a decoder

$F_1=\Sigma m(1,2,4,8,10,14)$, $f_2=\Sigma m(2,5,9,11)$, $f_3=\Sigma m(2,4,5,6,7)$

The minimum configuration of decoder will be _____

(1) 2 to 4 line

(2) 3 to 8 line

(3) 4 to 16 line

(4) 5 to 32 line

42. How many AND gates are required to realize Y=CD+EF+G?

(1) 4

(2) 5

(3) 3

(4) 2.

43. A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate?

(1) OR

(2) AND

(3) XOR

(4) NAND

44. A full adder logic circuit will have

(1) Two inputs and one output

(2) Three inputs and three outputs

(3) Two inputs and two outputs

(4) Three inputs and two outputs

45. How many two input AND gates and two input OR gates are required to realize $Y = BD + CE + AB$?

(1) 3,2

(2) 4,2

(3) 1,1

(4) 2,3

46. The gates required to build a half adder are _____

(1) EX-OR gate and NOR gate

(2) EX-OR gate and OR gate

(3) EX-OR gate and AND gate

(4) EX-NOR gate and AND gate

47. Which of the following is a type of digital logic circuit?

(1) Combinational logic circuits

(2) Sequential logic circuits

(3) Both Combinational & Sequential logic circuits

(4) None of the mentioned

48. When does a negative level triggered flip-flop in Digital Electronics changes its state?

(1) When the clock is negative

(2) When the clock is positive

(3) When the inputs are all zero

(4) When the inputs are all one

49. Which of the following options represent the synchronous control inputs in an S-R flip-flop?

(1) S

(2) R

(3) Clock

(4) Both S and R

50. What must be used along with synchronous control inputs to trigger a change in the flip-flop?

(1) 0

(2) 1

(3) Clock

(4) Previous output

51. What will be the output from a D flip-flop if the clock is low and D=0?

(1) 0

(2) 1

(3) No change

(4) Toggle between 0 and 1

52. What will be the output from a D flip-flop if D=1 and the clock is low?

(1) No change

(2) Toggle between 0 and 1

(3) 0

(4) 1

53. What value is [illegible] "don't care condition"?

(1) 0

(2) 1

(3) Either 0 or 1

(4) Any number except 0 and 1

54. What is the group of 16 in 4 variable K-map called?

(1) Pair

(2) Quad

(3) Octet

(4) Octave

55. How many entries will be in the truth table of a 4-input NAND gate?

(1) 6

(2) 8

(3) 32

(4) 16

56. In the toggle mode, a JK flip-flop has

(1) J=0, K=1

(2) J=1, K=1

(3) J=0, K=0

(4) J=1, K=0

57. A digital circuit that can store only one bit is a:

(1) Register

(2) NOR gate

(3) Flip-flop

(4) XOR gate

58. DeMorgan's Law states that:

(1) $(A+B)'=A'*B$

(2) $(AB)'=A'+B'$

(3) $(AB)'=A'+B$

(4) $(AB)'=A+B$

59. Algebra of logic is termed as _____

(1) Numerical logic

(2) Boolean algebra

(3) Arithmetic logic

(4) Boolean number

60. _____ value is represented by a Boolean expression.

(1) Positive

(2) Recursive

(3) Negative

(4) Boolean

61. Which of the following is a Simplification law?

(1) $M.(\sim M+N)=M.N$

(2) $M+(N.O)=(M+N)(M+O)$

(3) $\sim(M+N)=\sim M.\sim N$

(4) $M.(N.O)=(M.N).O$

62. What are the canonical forms of Boolean Expressions?

(1) OR and XOR

(2) NOR and XNOR

(3) MAX and MIN

(4) SOP and POS

63. The logic gate that provides high output for same inputs _____

(1) NOT

(2) X-NOR

(3) AND

(4) XOR

64. The _____ of all the variables in direct or complemented from is a maxterm.

(1) addition

(2) product

(3) modulo

(4) subtraction

65. What is computer organization?

(1) structure and behaviour of a computer system as observed by the user

(2) structure of a computer system as observed by the developer

(3) structure and behaviour of a computer system as observed by the developer

(4) All of the mentioned

66. To reduce the memory access time we generally make use of _____

(1) SDRAM's

(2) Heaps

(3) Cache Memory

(4) Higher capacity RAM's

67. The small extremely fast, RAM is known as _____

(1) Heaps

(2) Accumulators

(3) Stacks

(4) Cache

68. The memory devices which are similar to EEPROM but differ in the cost effectiveness is _____

(1) CMOS

(2) Memory sticks

(3) Blue-ray devices

(4) Flash memory

69. The drawback of building a large memory with DRAM is _____

(1) The Slow speed of operation

(2) The large cost factor

(3) The inefficient memory organization

(4) All of the mentioned

70. During a write operation if the required block is not present in the cache then ____ occurs.

(1) Write miss

(2) Write latency

(3) Write hit

(4) Write delay

71. PROM stands for _____:

(1) Programmable Read Only Memory

(2) Pre-fed Read Only Memory

(3) Pre-required Read Only Memory

(4) Programmed Read Only Memory

72. The PROM is more effective than ROM chips in regard to _____

(1) Cost

(2) Memory management

(3) Speed of operation

(4) Both Cost and Speed of operation

73. The ROM chips are mainly used to store _____

(1) System files

(2) Root directories

(3) Boot files

(4) Driver files

74. The contents of the EPROM are erased by _____

(1) Overcharging the chip

(2) Exposing the chip to UV rays

(3) Exposing the chip to IR rays

(4) Discharging the Chip

75. The disadvantage of the EPROM chip is _____

(1) The high cost factor

(2) The low efficiency

(3) The low speed of operation

(4) The need to remove the chip physically to reprogram it

Rough Work